WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a plurality of SRAM cells, each having a plurality of field effect transistors,

wherein each of said plurality of field effect transistors has a gate electrode thereof formed over a semiconductor substrate, a source region and a drain region formed in said semiconductor substrate, and a channel forming region formed in said semiconductor substrate and arranged between said source region and said drain region,

wherein a first field effect transistor selected from among said plurality of field effect transistors has a pair of semiconductor regions formed in said semiconductor substrate and serving as the source region and the drain region thereof such that end portions at a channel forming region side of said pair of semiconductor regions of said first field effect transistors are located in a direction away from opposite ends of the gate electrode of said first field effect transistor so as not be superposed with said gate electrode of said first field effect transistor, and

wherein said semiconductor integrated circuit device further comprises a second field effect transistor, which is formed on said semiconductor substrate and which is other than said first field effect transistor, said second field effect transistor having a pair of semiconductor regions formed in the semiconductor substrate and serving as the source region and the drain region thereof such that end portions at a channel forming region side of said pair of semiconductor regions are partially superposed with the gate electrode of said second filed effect transistor.

2. A semiconductor integrated circuit device according to claim 1, wherein a field effect transistor serving as a load of said SRAM cell is comprised of said first field effect transistor, and a field effect transistor for drive and selection of said SRAM cell is comprised of said second field effect transistor.

3. A semiconductor integrated circuit device according to claim 1, wherein said second field effect transistor comprises a field effect transistor of a peripheral circuit of the SRAM cells formed on said semiconductor substrate.

4. A semiconductor integrated circuit device according to claim 1, wherein said second field effect transistor comprises a field effect transistor of a logic circuit external to said SRAM cells.

5. A semiconductor integrated circuit device according to claim 1, wherein a plurality of said second field effect transistors comprise field effect transistors of a peripheral circuit of the SRAM cells and a logic circuit external to said SRAM cells.